WHAT IS CLAIMED IS:

1. A media processing system, comprising:

DRAM having a plurality of storage locations for storing digital data being processed by said media processing system, said digital data including video data that is compressed in a standardized format;

means for processing said digital data that includes said standardized format compressed video data to produce compressed video images and image data;

means for decoding said standardized format compressed video images to generate full motion video pixel data;

means for sharing said DRAM between said processing means and said decoding means; and

means for producing a full motion video signal from said full motion video pixel data.

2. The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said standardized compressed format comprises a luminance sample generated for each pixel, and two chrominance samples generated for every four pixels.

3. The system as recited in claim 2, wherein said decoding means comprises a Motion Picture Expert Group decoder.

4. The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for multiplying a first pixel with a second pixel in a single clock cycle of said processing means.

5. The system as recited in claim 4, wherein said pixels have a first portion, a second portion and a third portion, and said means for multiplying pixels comprises means for multiplying a portion of the first pixel with a corresponding portion of the second pixel.

6. The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for

combining a first pixel with a second pixel in a single clock cycle of said processing means.

7. The system as recited in claim 6, wherein said pixels have a first portion, a second portion and a third portion, and said means for combining pixels comprises means for combining a portion of the first pixel with a corresponding portion of the second pixel.

8. The system as recited in claim 1, wherein said processing means comprises a plurality of processing elements connected together in parallel, means for controlling said processing elements with instruction words that have a predetermined number of instructions, and means for distributing data simultaneously to each of said processing elements.

9. The system as recited in claim 8, wherein said processing elements comprise a plurality of processing units wherein each of said processing units is controlled by one of said predetermined number of instructions.

10. The system as recited in claim 1, wherein said DRAM stores audio data that is compressed in a standardized format, and further comprising means for decompressing said audio data that is compressed in a standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

11. The system as recited in claim 9, wherein said processing units comprise a plurality of storage locations within said processing units, each storage location having a predetermined physical size, and means for combining said storage locations together to form a storage location that stores data that is larger than the predetermined physical size of each storage location.

12. A single semiconductor chip media processor, comprising:

a semiconductor memory, internal to said single semiconductor chip, for storing digital data, including video digital data compressed in standardized format;

means for processing said compressed video data in said semiconductor memory to produce color, full motion video data that is temporarily stored in said semiconductor memory;

means for decoding said color, full motion video data stored in said semiconductor memory to generate color, full motion video image data; and

means for producing a color, full motion video image signal.

13. The processor as recited in claim 12, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for multiplying a first pixel with a second pixel in a single clock cycle of said processing means.

14. The processor as recited in claim 13, wherein said pixels have a first portion, a second portion and a third portion, and said means for multiplying pixels comprises means for multiplying a portion of the first pixel with a corresponding portion of the second pixel.

15. The processor as recited in claim 14, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for combining a first pixel with a second pixel in a single clock cycle of said processing means.

16. The processor as recited in claim 15, wherein said pixels have a first portion, a second portion and a third portion, and said means for combining pixels comprises means for combining a portion of the first pixel with a corresponding portion of the second pixel.

17. The processor as recited in claim 12, wherein said processing means comprises a plurality of processing elements connected together in parallel, means for controlling said processing elements with instruction words that have a predetermined number of instructions, and means for distributing data simultaneously to each of said processing elements.

18. The processor as recited in claim 17, wherein said processing elements comprise a plurality of processing units wherein each of said processing units is controlled by one of said predetermined number of instructions.

19. The processor as recited in claim 12, wherein said DRAM stores audio data that is compressed in a standardized format, and further comprising means for

decompressing said audio data that is compressed in a standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

20. The processor as recited in claim 18, wherein said processing units comprise a plurality of storage locations within said processing units, each storage location having a predetermined physical size, and means for combining said storage locations together to form a storage location that stores data that is larger than the predetermined physical size of each storage location.

21. A method of processing media, comprising:

storing digital data being processed by said media processing system in a DRAM, said digital data including video data that is compressed in a standardized format;

processing said digital data that includes said standardized format compressed video data to produce compressed video images and image data;

decoding said standardized format compressed video images to generate full motion video pixel data;

sharing said DRAM between said processing means and said decoding means; and

producing a full motion video signal from said full motion video pixel data.

22. The method as recited in claim 20, wherein said compressed video data comprises a plurality of pixels, and processing comprises multiplying a first pixel with a second pixel in a single clock cycle.

23. The method as recited in claim 21, wherein said compressed video data comprises a plurality of pixels, and processing comprises combining a first pixel with a second pixel in a single clock cycle.